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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,797	06/22/2001	Richard W. Adkisson	10012773-1	7649

7590 11/10/2005

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,797	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

The finality of the previous Office action is withdrawn.

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

The name " sampling compensation circuit" have not been given any weight other than what it is claimed: "a circuit operable to condition a SYNC pulse signal, wherein the SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion" as stated in claim 1. Also it appears that the sampling compensation circuit is shown in Fig 8A. The only description found uses the terminology of claim 1. Thought applicant is allowed to act as his own lexicographer, this is not done in this Application. Applicant does not define a sampling compensation circuit as something, so no inherent functionality can be inferred.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. Claim 10 is rejected because the specification doesn't disclose an "anomalous condition". Claims 11-13 are rejected because they depend from claim 10

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14-16 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Salmon (US 6662305).

As per claim 14, Salmon discloses a sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 3 column 3 lines 52-62); determining a clock state indicative of a phase difference between said first and second clock signals (figure 1 block 126 column 2 lines 41-53); re-positioning said SYNC pulse signal based on said clock state (figure 5 column 3 line 63 to column 4 line 27); and if said SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state (figure 6 block 610 column 5 line 55 to column 6 line 7).

As per claim 15, Salmon discloses claim 14. Elliot also discloses re-positioned by adding at least an extra clock cycle when said clock state indicates that said first clock signal lags with respect to said second clock signal by a predetermined amount (figure 5 302 column 3 line 63 to column 4 line 27).

As per claim 16, Salmon discloses claim 14. Elliot also discloses re-positioned by deleting at least an extra clock cycle when said clock state indicates that said second clock signal lags with respect to said first clock signal by a predetermined amount (figure 5 304 column 3 line 63 to column 4 line 27).

As per claim 19, Salmon discloses claim 14. Elliot also discloses a first and second clock signals comprise a core clock and a bus clock, respectively, in a computer system (abstract; figure1; figure2; figure 5 bus clock/PCI and host clock/CPU column 3 lines 7-18).

As per claim 20, Salmon discloses a sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion, wherein said SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal (figure 1 block 126 column 2 lines 41-53); and if said SYNC pulse signal is sampled to indicate a duplicate logic high condition during a predetermined time period, masking the duplicate logic high condition (figure 5 signal 304 column 3 line 63 to column 4 line 27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458) in view of Kurd (US 6622255), and further in view of Elliott (US 6826247).

As per claim 1, Price discloses a circuit operable to condition a SYNC pulse signal, wherein the SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, the jitter cycle delay compensation circuit operating to tap the SYNC pulse signal after a predetermined delay based on a skew difference between the first and second clock signals. Kurd discloses a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, the jitter cycle delay compensation circuit operating to delay the SYNC pulse signal after a predetermined delay based on a skew difference between the first and second clock signals (figure 6 column 5 lines 41-44). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit

disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Kurt doesn't specifically disclose that this delay compensation circuit is used to tap the signal. Elliot discloses a programmable delay circuit used to tap the signal (abstract; figure 2 block 202-204; column 5 lines 13-41). Kurd and Elliot teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate in the jitter compensation circuit disclosed by Kurd the tap delay disclosed by Elliot. The suggestion/motivation for doing so would have been to select at least one pulse at a precise point in the timing period (Elliot abstract). Therefore, it would have been obvious to combine Price, Kurd and Elliot to obtain the invention as specified in claim 1.

As per claim 5, Price, Kurd and Elliot disclose claim 1.Elliot also discloses a series of delay registers, each operating to delay the signal by a predetermined amount of time (figure 2 and figure 7 block 204; column 14 lines 7-26); and a multiplexer operable to select a delayed output generated from the series of delay registers (figure 2 and figure 7 block 206; column 14 lines 7-26).

As per claim 6, Price, Kurd and Elliot disclose claim 5.Elliot also discloses eight delay registers (figure 2 and figure 7 blocks 202 and 204; column 14 lines 7-26).

As per claim 7, Price, Kurd and Elliot disclose claim 5.Elliot also discloses that the multiplexer is actuated by a JITTER-STATE control signal generated by a

state/correct block responsive to skew differences between a first and second clock signals (figure 2 and figure 7 block 208; column 14 lines 7-26).

As per claim 8, Price, Kurd and Elliot disclose claim 7.Elliot also discloses that state/correct block is coupled to a phase detector operating to detect said skew difference between a first and second clock signals (figure 2 and figure 7 block 208; column 14 lines 7-26)

As per claim 9, Price, Kurd and Elliot disclose claim 7.Elliot also discloses that the control signal is stored in a flip-flop (figure 3 block 316; column 9 lines 8-26)

Claims 1 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmon (US 6662305) in view of Kurd (US 6622255), and further in view of Elliott (US 6826247).

As per claim 1, Salmon discloses a circuit operable to condition a SYNC pulse signal, wherein the SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 3 column 3 lines 52-62). Salmon doesn't disclose a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, the jitter cycle delay compensation circuit operating to tap the SYNC pulse signal after a predetermined delay based on a skew difference between the first and second clock signals. Kurd discloses a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, the jitter cycle delay compensation circuit operating to delay the SYNC pulse signal after a predetermined delay based on a skew difference between the first and second clock signals (figure 6

column 5 lines 41-44). Salmon and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with the SYNC pulse signal disclosed by Salmon. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Kurt doesn't specifically disclose that this delay compensation circuit is used to tap the signal. Elliot discloses a programmable delay circuit used to tap the signal (abstract; figure 2 block 202-204; column 5 lines 13-41). Kurd and Elliot teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate in the jitter compensation circuit disclosed by Kurd the tap delay disclosed by Elliot. The suggestion/motivation for doing so would have been to select at least one pulse at a precise point in the timing period (Elliot abstract). Therefore, it would have been obvious to combine Salmon, Kurd and Elliot to obtain the invention as specified in claim 1.

As per claim 5, Salmon, Kurd and Elliot disclose claim 1.Elliot also discloses a series of delay registers, each operating to delay the signal by a predetermined amount of time (figure 2 and figure 7 block 204; column 14 lines 7-26); and a multiplexer operable to select a delayed output generated from the series of delay registers (figure 2 and figure 7 block 206; column 14 lines 7-26).

As per claim 6, Salmon, Kurd and Elliot disclose claim 5.Elliot also discloses eight delay registers (figure 2 and figure 7 blocks 202 and 204; column 14 lines 7-26).

As per claim 7, Salmon, Kurd and Elliot disclose claim 5.Elliot also discloses that the multiplexer is actuated by a JITTER-STATE control signal generated by a state/correct block responsive to skew differences between a first and second clock signals (figure 2 and figure 7 block 208; column 14 lines 7-26).

As per claim 8, Salmon, Kurd and Elliot disclose claim 7.Elliot also discloses that state/correct block is coupled to a phase detector operating to detect said skew difference between a first and second clock signals (figure 2 and figure 7 block 208; column 14 lines 7-26)

As per claim 9, Salmon, Kurd and Elliot disclose claim 7.Elliot also discloses that the control signal is stored in a flip-flop (figure 3 block 316; column 9 lines 8-26).

As per claim 14, Salmon discloses a sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 3 column 3 lines 52-62); determining a clock state indicative of a phase difference between said first and second clock signals (figure 1 block 126 column 2 lines 41-53); re-positioning said SYNC pulse signal based on said clock state (figure 5 column 3 line 63 to column 4 line 27); and if said SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state (figure 6 block 610 column 5 line 55 to column 6 line 7).

Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmon (US 6662305) in view Elliott (US 6826247).

As per claim 17, Salmon discloses claim 14. Salmon doesn't specifically disclose delaying by propagating the signal through a series of delay registers operable to be selected by a multiplexer in response to a JITTER-STATE control signal corresponding to the clock state. Elliott discloses delaying by propagating the signal through a series of delay registers operable to be selected by a multiplexer in response to a JITTER-STATE control signal corresponding to the clock state (figure 2 blocks 202, 204, 206 and 208 column 6 lines 16-60). Salmon and Elliot teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate in the synchronization circuit disclosed by Salmon the tap delay disclosed by Elliot. The suggestion/motivation for doing so would have been to select at least one pulse at a precise point in the timing period (Elliot abstract). Therefore, it would have been obvious to combine Salmon and Elliot to obtain the invention as specified in claim 17.

As per claim 18, Salmon and Elliott disclose claim 17. Elliott also discloses that the JITTER-STATE control signal is stored in at least one flip-flop (figure 3 block 316; column 9 lines 8-26).

Allowable Subject Matter

The indicated allowability of claims 13 and 20 is withdrawn in view of the newly discovered reference(s) to Salmon (US 6662305. Rejections based on the newly cited reference(s) follow.

Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: claims 2-4 are allowed because the references cited fail to teach, as applicant has, a SYNC pulse compensation circuit comprising a plurality of multiplexers arranged in series, each multiplexer operating to receive an input through a timing register associated therewith, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
11-07-2005

KEVIN BURD
PRIMARY EXAMINER